a dielectric layer situated over the semiconductor body and contacting the body region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage being maintained approximately constant at a non-zero value as the plate-to-body voltage is varied.

18. (Original) A structure as in Claim 17 further including componentry for maintaining the gate-to-body voltage approximately constant at the non-zero value.

19. (Original) A structure as in Claim 17 wherein the plate and body regions extend to a primary surface of the semiconductor body.

20. (Previously amended) A structure as in Claim 19 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode under control of the plate and body electrodes, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

21. (Original) A structure as in Claim 19 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region.

22. (Original) A structure as in Claim 21 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

23. (Previously amended) A structure comprising a varactor which comprises:

a plate region and a body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode;

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

a dielectric layer situated over the semiconductor body and contacting the body region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage differing from the plate-to-body voltage, the gate-to-body voltage varying as a function of the plate-to-body voltage as the plate-to-body voltage is varied during operation of the varactor to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

24. (Original) A structure as in Claim 23 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

25. (Original) A structure as in Claim 23 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

26. (Original) A structure as in Claim 23 further including componentry for causing the gate-to-body voltage to vary as a function of the plate-to-body voltage.

27. (Original) A structure as in Claim 26 wherein the componentry causes the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.

28. (Original) A structure as in Claim 23 wherein the plate and body regions extend to a primary surface of the semiconductor body.

29. (Previously amended) A structure as in Claim 28 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

30. (Original) A structure as in Claim 28 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region.

31. (Previously amended) A structure as in Claim 30 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion,

extending laterally away from the main plate portion, and meeting the body region therealong.

32. (Previously amended) A structure comprising:

a plate region and a body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions extending to a primary surface of the semiconductor body and meeting each other to form a p-n junction, the plate region comprising a main plate portion and a plurality of finger portions continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong, at least two of the finger portions extending longitudinally non-parallel to one another;

a dielectric layer situated over the semiconductor body and contacting the plate region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region.

33. (Previously amended) A structure as in Claim 32 wherein each finger portion is of lesser average dimension perpendicular to that finger portion than is the main plate portion.

34. (Previously amended) A structure as in Claim 32 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region including each finger portion.

35. (Original) A structure as in Claim 32 further including a field insulating region extending into the semiconductor body along its primary surface, the field insulating region laterally adjoining the body region.

36. (Previously amended) A structure as in Claim 32 wherein two of the finger portions extend longitudinally largely perpendicular to each other.

37. (Original) A structure as in Claim 32 wherein there are at least four finger portions.

38. (Previously amended) A method comprising:

selecting a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a dielectric layer situated over the semiconductor body and

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

contacting the body region, (c) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, and (d) a plate electrode and a body electrode respectively connected to the plate and body regions, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region selectively appearing and disappearing in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and body electrodes is varied during operation of the varactor, the inversion layer occupying a lateral inversion area along the primary surface, the varactor having a maximum capacitance dependent on the inversion area in combination with the plate area; and

adjusting the plate and inversion areas to control the minimum and maximum capacitances of the varactor.

39. (Original) A method as in Claim 38 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to an accumulative combination of the inversion and plate areas.

40. (Original) A method as in Claim 38 wherein the adjusting step involves adjusting the ratio of the inversion area to the plate area in order to achieve at least a specified value of the ratio of the maximum capacitance to the minimum capacitance.

41. (Previously amended) A method as in Claim 38 wherein the selecting act includes configuring the body region to substantially laterally surround, and extend below substantially all of, the plate region.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

42. (Previously amended) A method as in Claim 38 wherein the selecting and adjusting acts include configuring the plate region to comprise a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

43. (Previously amended) A method as in Claim 38 wherein the gate electrode is at a gate-to-body bias voltage relative to the body electrode, the method further including

maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

44. (Previously amended) A method as in Claim 38 wherein the gate electrode is at gate-to-body bias voltage relative to the body electrode, the method further including causing the gate-to-body voltage to differ from the plate-to-body voltage and to vary as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

45. (Original) A method as in Claim 44 wherein the causing act entails causing the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.

46. (Original) A method as in Claim 44 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

47. (Previously presented) A structure as in Claim 17 further including electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

48. (Previously presented) A structure as in Claim 47 wherein the gate electrode is situated outside the capacitance signal path.

49. (Previously presented) A structure as in Claim 47 wherein the circuitry comprises at least one additional region of the semiconductor body.

50. (Previously presented) A structure as in Claim 47 wherein the circuitry comprises an inductor.

51. (Previously presented) A structure as in Claim 17 further including electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

52. (Previously presented) A structure as in Claim 51 wherein the gate electrode is situated outside the inductance-capacitance signal path.

53. (Previously presented) A structure as in Claim 17 wherein a surface depletion region of the body region extends along the dielectric layer below the gate electrode and is spaced

apart from a body contact portion of the body region, the body contact portion contacting the body electrode and being more heavily doped than the surface depletion region.

54. (Currently amended) A structure as in Claim 22 wherein each finger portion is of lesser average dimension perpendicular to that finger portion than is the main plate portion.

55. (Previously presented) A structure as in Claim 23 further including electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

56. (Previously presented) A structure as in Claim 55 wherein the gate electrode is situated outside the capacitance signal path.

57. (Previously presented) A structure as in Claim 55 wherein the circuitry comprises at least one additional region of the semiconductor body.

58. (Previously presented) A structure as in Claim 55 wherein the circuitry comprises an inductor.

59. (Previously presented) A structure as in Claim 23 further including electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

60. (Previously presented) A structure as in Claim 59 wherein the gate electrode is situated outside the inductance-capacitance signal path.

61. (Previously presented) A structure as in Claim 23 wherein a surface depletion region of the body region extends along the dielectric layer below the gate electrode and is spaced apart from a body contact portion of the body region, the body contact portion contacting the body electrode and being more heavily doped than the surface depletion region.

62. (Currently amended) A structure as in Claim 31 wherein each finger portion is of lesser average dimension perpendicular to that finger portion than is the main plate portion.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

63. (Previously presented) A structure comprising:

a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction, a surface depletion region of the body region extending along the dielectric layer below the gate electrode and being spaced apart from a body contact portion of the body region, the body contact portion contacting the body electrode and being more heavily doped than the surface depletion region, the plate region comprising a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong; and

electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

64. (Previously amended) A structure as in Claim 63 wherein each finger portion is of lesser average dimension perpendicular to that finger portion than is the main plate portion.

65. (Previously presented) A structure as in Claim 63 wherein there are at least two finger portions.

66. (Previously presented) A structure as in Claim 63 wherein there are at least four finger portions.

67. (Previously presented) A structure as in Claim 63 wherein the varactor includes a plate electrode and a body electrode respectively connected to the plate and body regions, an inversion layer that meets the plate region selectively appearing and disappearing in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and body electrodes is varied during operation of the varactor.

68. (Previously presented) A structure as in Claim 65 wherein at least two of the finger portions extend longitudinally non-parallel to another.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

69. (Previously presented) A structure as in Claim 17 wherein an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode as the plate-to-body voltage is varied during operation of the varactor.

70. (Previously presented) A structure as in Claim 32 further including a plate electrode and a body electrode respectively connected to the plate and body regions, an inversion layer that meets the plate region selectively appearing and disappearing in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and the body electrodes is varied during operation of the structure.

71. (Previously presented) A method comprising:

providing a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

applying (a) a plate-to-body bias voltage between the plate and body electrodes and (b) a gate-to-body bias voltage between the gate and body electrodes; and

varying the plate-to-body voltage while maintaining the gate-to-body voltage approximately constant at a non-zero value to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

72. (Previously presented) A method as in Claim 71 further including providing componentry for maintaining the gate-to-body voltage approximately constant at the non-zero value.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

73. (Previously presented) A method as in Claim 71 wherein the plate and body regions extend to a primary surface of the semiconductor body, the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

74. (Previously presented) A method as in Claim 71 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

75. (Previously presented) A method as in Claim 71 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

76. (Previously presented) A method as in Claim 75 wherein the gate electrode is situated outside the capacitance signal path.

77. (Previously presented) A method as in Claim 71 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

78. (Previously presented) A method as in Claim 77 wherein the gate electrode is situated outside the inductance-capacitance signal path.

79. (Previously presented) A method comprising:

providing a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

applying (a) a plate-to-body bias voltage between the plate and body electrodes and (b) a gate-to-body bias voltage between the gate and body electrodes; and

varying (a) the plate-to-body voltage and (b) the gate-to-body voltage as a function of the plate-to-body voltage as the plate-to-body voltage is varied to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

80. (Previously presented) A method as in Claim 79 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

81. (Previously presented) A method as in Claim 79 further including providing componentry for causing the gate-to-body voltage to vary as a function of the plate-to-body voltage.

82. (Previously presented) A method as in Claim 79 wherein the componentry causes the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.

83. (Previously presented) A method as in Claim 79 wherein the plate and body regions extend to a primary surface of the semiconductor body, the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

84. (Previously presented) A method as in Claim 79 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

85. (Previously presented) A method as in Claim 79 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

86. (Previously presented) A method as in Claim 85 wherein the gate electrode is situated outside the capacitance signal path.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

87. (Previously presented) A method as in Claim 79 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

88. (Previously presented) A method as in Claim 87 wherein the gate electrode is situated outside the inductance-capacitance signal path.

89. (Previously presented) A method as in Claim 71 wherein:

the plate and body regions extend to a primary surface of the semiconductor body; and

the providing act includes providing a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions.

90. (Previously presented) A method as in Claim 89 wherein the providing act includes configuring the plate region to be a substantially unitary region.

91. (Previously presented) A method as in Claim 89 wherein the providing act includes configuring the field insulating region to substantially laterally surround at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

92. (Previously presented) A method as in Claim 79 wherein:

the plate and body regions extend to a primary surface of the semiconductor body; and

the providing act includes providing a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions.

93. (Previously presented) A method as in Claim 92 wherein the providing act includes configuring the plate region to be a substantially unitary region.

94. (Previously presented) A method as in Claim 92 wherein the providing act includes configuring the field insulating region to substantially laterally surround at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

95. (Previously presented) A method comprising:

selecting a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a dielectric layer situated over the semiconductor body and contacting the body region, (c) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, and (d) a plate electrode and a body electrode respectively connected to the plate and body regions, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions, the semiconductor island occupying a lateral island area along the primary surface, the varactor having a maximum capacitance dependent on the island area; and

adjusting the plate and island areas to control the minimum and maximum capacitances of the varactor.

96. (Previously presented) A method as in Claim 95 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to the island area.

97. (Previously presented) A method as in Claim 95 wherein the selecting act includes configuring the plate region to be a substantially unitary region.

98. (Previously presented) A method as in Claim 95 wherein the selecting act includes configuring the field insulating region to substantially laterally surround at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

99. (Previously presented) A method as in Claim 95 wherein the selecting and adjusting acts include configuring the plate region to comprise a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

100. (Previously presented) A method as in Claim 95 wherein an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and body electrodes is varied during operation of the varactor.

101. (Previously presented) A method as in Claim 95 wherein the gate electrode is at a gate-to-body bias voltage relative to the body electrode, the method further including maintaining the gate-to-body voltage approximately constant at a non-zero value as the plate-to-body voltage is varied.

102. (Previously presented) A method as in Claim 95 wherein the gate electrode is at gate-to-body bias voltage relative to the body electrode, the method further including causing the gate-to-body voltage to differ from the plate-to-body voltage and to vary as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

103. (Previously presented) A method as in Claim 102 wherein the causing act entails causing the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.

104. (Previously presented) A method as in Claim 102 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

105. (Previously presented) A method as in Claim 95 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

106. (Previously presented) A method as in Claim 105 wherein the gate electrode is situated outside the capacitance signal path.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

107. (Previously presented) A method as in Claim 95 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

108. (Previously presented) A method as in Claim 107 wherein the gate electrode is situated outside the inductance-capacitance signal path.

109. (Previously presented) A structure comprising:

a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions; and

electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

110. (Previously presented) A structure as in Claim 109 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the semiconductor island occupies a lateral island area along the primary surface, and the varactor has a maximum capacitance dependent on the island area.

111. (Previously presented) A method as in Claim 110 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to the island area.

112. (Previously presented) A structure as in Claim 109 wherein the plate region is a substantially unitary region.

113. (Previously presented) A structure as in Claim 109 wherein the field insulating region substantially laterally surrounds at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

114. (Previously presented) A structure as in Claim 109 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

115. (Previously presented) A structure as in Claim 109 wherein an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and body electrodes is varied during operation of the varactor.

116. (Previously presented) A structure as in Claim 109 wherein the plate electrode is at a plate-to-body bias voltage relative to the body electrode, the gate electrode is at a gate-to-body bias voltage relative to the body electrode, and the gate-to-body voltage is maintained approximately constant as the plate-to-body voltage is varied.

117. (Previously presented) A structure as in Claim 109 wherein the plate electrode is at a plate-to-body bias voltage relative to the body electrode, the gate electrode is at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage differs from the plate-to-body voltage, and the gate-to-body voltage is varied as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

118. (Previously presented) A structure as in Claim 117 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

119. (Previously presented) A structure as in Claim 117 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

120. (Previously presented) A structure as in Claim 109 wherein the gate electrode is situated outside the capacitance signal path.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

121. (Previously presented) A structure as in Claim 109 wherein the circuitry includes an inductor situated in the capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination whereby the capacitance signal path is an inductance-capacitance signal path.

122. (Previously presented) A structure as in Claim 121 wherein the gate electrode is situated outside the inductance-capacitance signal path.

123. (New) A structure as in Claim 19 further including a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions.

124. (New) A structure as in Claim 123 wherein the plate region is a substantially unitary region.

125. (New) A method as in Claim 123 wherein the field insulating region substantially laterally surrounds at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

126. (New) A structure as in Claim 28 further including a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions.

127. (New) A structure as in Claim 126 wherein the plate region is a substantially unitary region.

128. (New) A method as in Claim 126 wherein the field insulating region substantially laterally surrounds at least one further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

129. (New) A structure as in Claim 116 further including componentry for maintaining the gate-to-body voltage approximately constant at the non-zero value.

130. (New) A structure as in Claim 117 further including componentry for causing the gate-to-body voltage to vary as a function of the plate-to-body voltage.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779